through said first conductor plugs to electrically connect said second and third semiconductor regions to one another through said second conductive strip;

a second insulating film formed over said first insulating film and said first and second conductive strips;

a second opening formed in said second insulating film over an upper surface of one of the first conductor plugs formed in one of said first openings in the first insulating film and connected to the other of said first semiconductor regions of said MISFET;

a second conductor plug formed in said second opening in said second insulating film to electrically connect with said one of said first conductor plugs connected to the other of said first semiconductor regions of said MISFET; and

a third conductive strip formed on said second insulating film and electrically connected to said second conductor plug;

wherein one of first conductor plugs is directly physically connected to one of the first semiconductor regions and the first conductive strip in said first portion and another of the first conductor plugs is directly physically connected to one of the second semiconductor regions and the second conductive strip in the second portion.

REMARKS

Reconsideration and allowance of this application, as amended, is respectfully requested.

The present amendment is filed to further clarify the invention over the cited prior art, based upon discussions during a interview with the Examiner on September 5, 2002. Applicants and the undersigned attorney greatly appreciate the

courteousness and helpful comments provided by Examiner Pompey during the above-noted interview.

By the present amendment, each of the independent claims 42 and 47 has been amended to further clarify distinctions over the cited reference to Chu, USP 5,783,471. Specifically, each of these claims has been amended to define:

> "wherein one of first conductor plugs is directly physically connected to one of the first semiconductor regions and the first conductive strip in said first portion and another of the first conductor plugs is directly physically connected to one of the second semiconductor regions and the second conductive strip in the second portion."

For an appreciation of this, references made to the sketch which was provided with the September 3, 2002 amendment, a copy of which is attached herewith. As can be appreciated from this sketch, one of the first conductor plugs is physically connected to both a first semiconductor region and the first conductive strip in the first portion of the semiconductor device. Another of the first conductor plugs is physically connected to a second semiconductor region and a second conductive strip in the second portion of the device.

It is noted that the reference to Chu fails to teach or suggest this newly added feature concerning the physical connections of the first conductor plugs to the respective semiconductor regions and conductive strips. On the contrary, referring to Fig. 3V of the Chu reference, discussed during the above-noted interview, it can be seen that Chu shows two stacked plugs 310B and 315 formed in a first insulating film 312 and connected to a semiconductor region 305B and a first conductive strip 316 formed over the top of the stacked plug 315. On the other hand, a long single plug 313 is formed in the same insulating film 312 and connected to the semiconductor region 332 and a conductive strip 317. As such, the recited physical

connection does not exist between the plug 310B and the first conductive strip 316. Similarly, the recited physical connection does not exist between the plug 315 and the first semiconductor region (e.g., 305B). As such, the claimed relationship of direct physical contact between the first conductor plugs and semiconductor regions and conductive strips is not found in the Chu reference. As a result of the differences between Chu and the present claimed invention, the aspect ratio of the openings such as 333 in Chu (e.g., see Fig. 3U) is quite large. This results in further structural differences between Chu and the present claimed invention, and the inability to achieve the advantages of a structure constructed in accordance with the present claims. Therefore, reconsideration and allowance of amended independent claims 42-47 and the dependent claims is respectfully requested.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached page is captioned "Version with markings to show changes made."

If the Examiner believes that there are any other points which may be clarified or otherwise disposed of, either by telephone discussion or by personal interview, the Examiner is invited to contact applicants' undersigned attorney at the number indicated below.

To the extent necessary, the applicants petition for an extension of time under 37 CFR 1.136. Please charge any shortage in the fees due in connection with the

filing of this paper, including extension of time fees, to the deposit account of Antonelli, Terry, Stout & Kraus, Deposit Account No. 01-2135 (501.35437CV2).

Respectfully submitted,

ANTONELLI, TERRY, STOUT & KRAUS, LLP

By _____
Gregory E. Montone
Registration No. 28,141

GEM/kd
703/312-6600

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the Claims:

Claims 42 and 47 have been amended as follows:

42. (Amended) A semiconductor integrated circuit device having a first portion for a memory array and a second portion for a circuit other than the memory array on a semiconductor substrate comprising:

a MISFET arranged in said first portion, said MISFET having first semiconductor regions and a gate electrode between said first semiconductor regions;

second semiconductor regions arranged in said second portion;

a first insulating film formed over said semiconductor substrate to cover said first and second portions;

a plurality of first openings formed simultaneously in said first insulating film above both said first and second portions;

a plurality of first conductor plugs formed in said first openings in said first insulating film on said first semiconductor regions in said first portion and on said second semiconductor regions in said second portion;

a first conductive strip formed on said first insulating film in said first portion and electrically connected to one of the first semiconductor regions of said MISFET through one of said first conductor plugs; and

a second conductive strip formed on said first insulating film in said second portion and electrically connected to said second semiconductor regions through said first conductor plugs to electrically connect said second semiconductor regions

to one another through said second conductive strip;

a second insulating film formed over said first insulating film and said first and second conductive strips;

a second opening formed in said second insulating film over an upper surface of one of the first conductor plugs formed in one of said first openings in the first insulating film and connected to the other of said first semiconductor regions of said MISFET;

a second conductor plug formed in said second opening in said second insulating film to electrically connect with said one of said first conductor plugs connected to the other of said first semiconductor regions of said MISFET; and

a third conductive strip formed on said second insulating film and electrically connected to said second conductor plug[.],

wherein one of first conductor plugs is directly physically connected to one of the first semiconductor regions and the first conductive strip in said first portion and another of the first conductor plugs is directly physically connected to one of the second semiconductor regions and the second conductive strip in the second portion.

47. (Amended) A semiconductor integrated circuit device having a first portion for a memory array and a second portion for a circuit other than the memory array on a semiconductor substrate comprising:

a MISFET arranged in said first portion, said MISFET having first semiconductor regions of n-type conductivity and a gate electrode between said first semiconductor regions;

a second semiconductor region of n-type conductivity and a third

semiconductor region of p-type conductivity arranged in said second portion;

a first insulating film formed over said semiconductor substrate to cover said first and second portions;

a plurality of first openings formed simultaneously in said first insulating film above both said first and second portions;

a plurality of first conductor plugs each comprising a tungsten film formed in said first openings in said first insulating film on said first semiconductor regions in said first portion and on said second semiconductor regions in said second portion;

a first conductive strip formed on said first insulating film in said first portion and electrically connected to one of the first semiconductor regions of said MISFET through one of said first conductor plugs; and

a second conductive strip formed on said first insulating film in said second portion and electrically connected to said second and third semiconductor regions through said first conductor plugs to electrically connect said second and third semiconductor regions to one another through said second conductive strip;

a second insulating film formed over said first insulating film and said first and second conductive strips;

a second opening formed in said second insulating film over an upper surface of one of the first conductor plugs formed in one of said first openings in the first insulating film and connected to the other of said first semiconductor regions of said MISFET;

a second conductor plug formed in said second opening in said second insulating film to electrically connect with said one of said first conductor plugs connected to the other of said first semiconductor regions of said MISFET; and

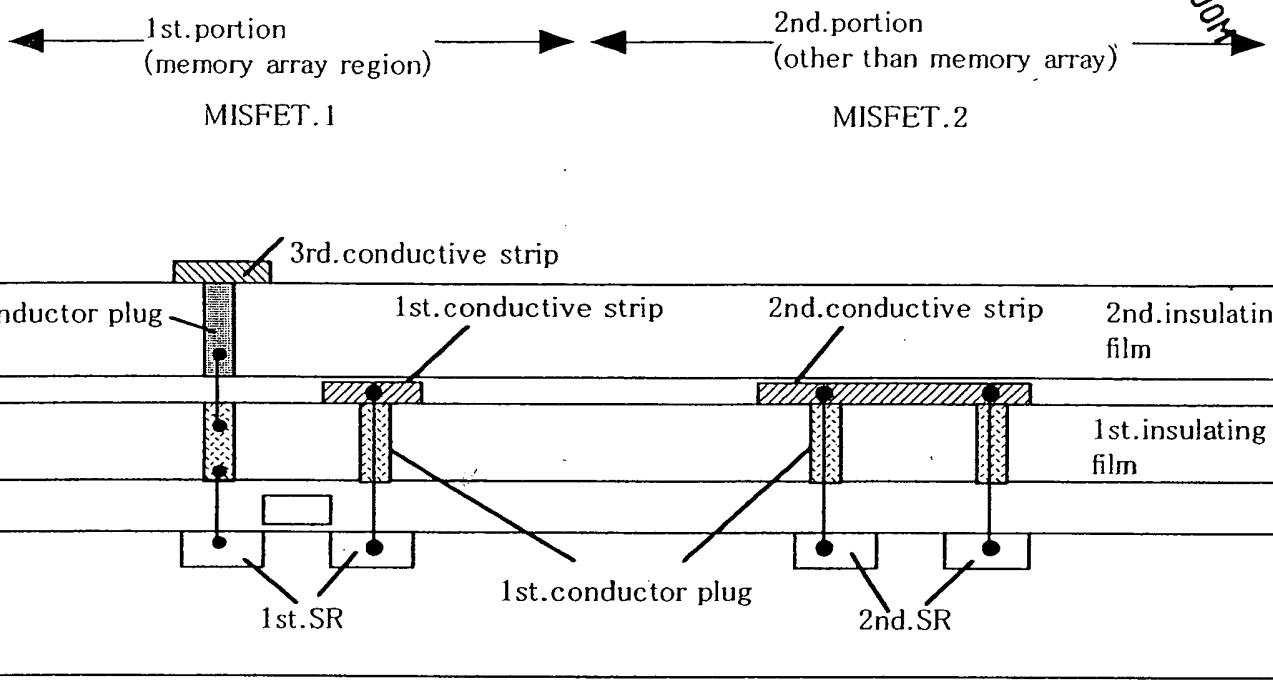
a third conductive strip formed on said second insulating film and electrically

connected to said second conductor plug[.],

wherein one of first conductor plugs is directly physically connected to one of the first semiconductor regions and the first conductive strip in said first portion and another of the first conductor plugs is directly physically connected to one of the second semiconductor regions and the second conductive strip in the second portion.

【代理人提案クレーム】

42.



43. 1st. conductor plug : W

44. 1st. conductor plug : TiN/W

45. 2nd.SRs : P-type & N-type

46. 2nd.conductor plug : W

Comparison between claim 42 and prior art

	claim 42	prior art (USP5,783,471)	differences between claim 42 and prior art
memory array	1st.conductor plug	plugs (310A,310B)	
	1st.insulating film	insulating film (BPSG)	
	1st.conductor strip	-	
	2nd.conductor plug	plug (314,315)	2nd.conductor plug is formed in the 2nd.insulating film. Plug (314,315) is formed in insulating film (BPSG).
	2nd.insulating film	-	
	3rd.conductor strip	AL bit line (316)	3rd.conductor strip is formed on 2nd.insulating film. AL bit line(316) is formed on insulating film BPSG).
peripheral circuit	1st.conductor plug	plug (313)	1st.conductor plug in peripheral circuit is formed as the same step of forming the 1st.conductor plug in memory array rgion. Plug (313) is formed as the same step of plug (314,315).
	2nd.conductor strip	wiring (317)	

In claim 42, each plug is formed in each inter-layer insulating film, for exmple, a first plug is formed in a first insulating film and a second plug is formed in a second insulating film.

Therefore aspect ration of connecting hole is not so large in comparison to the prior art. Assuming that an insulating film (BPSG) includes the first and second insulating film of claim 42, the aspect ration of connecting hole formed plug (313) is large, because such connecting hole is formed in two layer of interlayer insulating film.